WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

first, second and third power supply conductors, wherein the second power supply conductor has a higher voltage than the first power supply conductor and the third power supply conductor has a higher voltage than the second power supply conductor;

a high voltage power supply decoupling capacitor coupled between the first and third power supply conductors;

a low voltage power supply decoupling capacitor coupled between the first and second power supply conductors;

a voltage reducer coupled between the second and third power supply conductors; and

a core circuit portion formed of a plurality of semiconductor devices, which are biased between the first and second power supply conductors.

2. The integrated circuit of claim 1 and further comprising:

a die comprising the first, second and third power supply conductors, the high and low power supply decoupling capacitors, the voltage reducer and the core circuit portion; and

a package comprising a high voltage power supply pin electrically coupled to the third power supply conductor, and a ground power supply pin electrically coupled to the first power supply conductor.

3. The integrated circuit of claim 2 wherein the package further comprises:

a low voltage power supply pin electrically coupled to the second power supply conductor, which has a voltage that is higher than the ground power supply pin and lower than the high voltage power supply pin.

4. The integrated circuit of claim 3 wherein the voltage reducer comprises a reference voltage input, which is coupled to the low voltage power supply pin.

5. The integrated circuit of claim 1 wherein the voltage reducer comprises a switching type of voltage regulator, which selectively couples charge from the high voltage power supply decoupling capacitor to the low voltage power supply decoupling capacitor when the voltage between the first and second power supply conductors drops below a reference voltage.

6. The integrated circuit of claim 1 wherein the high voltage power supply decoupling capacitor has a higher breakdown voltage than the low voltage power supply decoupling capacitor.

7. The integrated circuit of claim 1 wherein the high voltage power supply decoupling capacitor comprises a parallel-plate, metal-insulator-metal (MIM) capacitor.

8. The integrated circuit of claim 7 wherein the high voltage power supply decoupling capacitor comprises at least one insulator layer that has a higher dielectric constant than corresponding insulator layers in the core circuit portion.

9. The integrated circuit of claim 1 wherein the low voltage power supply decoupling capacitor comprises a plurality of parallel-connected metal oxide semiconductor gate capacitances.

10. An integrated circuit comprising:

a package comprising first, second and third power supply pins, wherein the second pin has a higher voltage than the first pin and the third pin has a higher voltage than the second pin;

a die comprising first, second, and third power supply conductors, which are coupled to the first, second and third power supply pins, respectively;

a low voltage power supply decoupling capacitor on the die and coupled between the first and second power supply conductors;

a plurality of semiconductor devices on the die, which are biased between the first and second power supply conductors;

a high voltage power supply decoupling capacitor on the die and coupled between the first and third power supply conductors; and

a voltage reducer on the die and coupled between the second and third power supply conductors.

11. The integrated circuit of claim 10 wherein the voltage reducer comprises a reference voltage input, which is coupled to the second power supply pin.

12. The integrated circuit of claim 10 wherein the voltage regulator comprises a switching type of voltage regulator, which selectively couples charge from the high voltage power supply decoupling capacitor to the low voltage power supply decoupling capacitor when the voltage between the first and second power supply conductors drops below a reference voltage.

13. The integrated circuit of claim 10 wherein the high voltage power supply decoupling capacitor has a higher breakdown voltage than the low voltage power supply decoupling capacitor.

14. The integrated circuit of claim 10 wherein the high voltage power supply decoupling capacitor comprises a parallel-plate, metal-insulator-metal (MIM) capacitor.

15. The integrated circuit of claim 14 wherein the high voltage power supply decoupling capacitor comprises at least one insulator layer that has a higher dielectric constant than corresponding insulator layers fabricated within a core region of the die.

16. The integrated circuit of claim 10 wherein the low voltage power supply decoupling capacitor comprises a plurality of parallel-connected metal oxide semiconductor gate capacitances.

17. An integrated circuit die comprising:

first, second, and third power supply conductors, wherein the second power supply conductor has a higher voltage than the first power supply conductor and the third power supply conductor has a higher voltage than the second power supply conductor;

a low voltage power supply decoupling capacitor coupled between the first and second power supply conductors;

a plurality of semiconductor devices, which are biased between the first and second power supply conductors;

a high voltage power supply decoupling capacitor coupled between the first and third power supply conductors; and

charge coupling means coupled between the second and third power supply conductors for selectively coupling charge from the high voltage power supply decoupling capacitor to the low voltage power supply decoupling capacitor when the voltage between the first and second power supply conductors drops below a reference voltage.